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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
PIERRE LOUIS, ANDRE	
ART UNIT	PAPER NUMBER
2123	

DATE MAILED: 01/10/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/037,191	SCHULTER ET AL.	
	Examiner	Art Unit	
	Andre Pierre-Louis	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 October 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1.0 The amendment filed on 10/26/2005 have been received and considered, claims 1-20 are presented for evaluation.

Response to Arguments

2.0 Applicant's arguments filed 10/26/2005 have been fully considered but they are not persuasive.

2.1 Applicant argues that Aditya, Hebert, and Trachewsky alone or in combination do not teach an Ethernet emulation, the examiner agrees and relies Cox et al. teachings of an emulated LAN and that host attached to the ELAN teaches by Cox et al. includes emulation software that allows them to emulate LAN (col.2 lines 55-66; also col.8 lines 22-42). Therefore the combined teachings of Cox et al., Aditya, Hebert, and Trachewsky et al. teach the emulated Ethernet as set forth below in the new ground of rejection.

2.2 Applicant argues that Hebert teachings do not pertain to switching, the examiner respectfully disagrees and relies on fig.6-9, 13; also col.8 line 38-col.12 line 2.

2.3 Applicant argues that there is no bypassing for the network switch teaches by Aditya, the examiner relies on Cox et al. col.3 line 53-col.4 line 25, as set forth below in the new ground of rejection.

2.4 With regards to the added limitations in the amended claims, the examiner does consider these added limitations to be novel and a rejection is set forth below.

2.5 While the applicant believes that the claims should be found allowable, the examiner respectfully disagrees and relies on the new ground of rejection as set forth below.

Claim Rejections - 35 USC § 112

3.0 Claims 1-20 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter, which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. While claiming a non-Ethernet switch fabric, the specification merely refers to a switch fabric.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

4.0 Claims 1-4,9 and 11-14,19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cox et al. (*U.S. Patent No. 6,189,041*), in view of Aditya (*U.S. Patent No. 5,918,021)*.

4.1 In considering the independent claims 1 and 11, Cox et al. substantially teaches a method of emulating a switched Ethernet local area network in a computing platform having a plurality of computer processors, a non-Ethernet switch fabric with point-to-point links between the non-Ethernet switch and the computer processors and particularly teaches the steps of: defining a switched Ethernet network topology of to be emulated on the computing platform, the topology including processor nodes and a switch node (*col.2 line 1-col.3 line 66*); assigning a set of computer processors to act as the processor nodes (*col.5 line 26-col.6 line 59*); assigning a computer processor to act as the switch node, said switch node emulating an Ethernet switch (*col.7 line 7-col.9 line 18*); however, he does not expressly teaches providing Ethernet driver emulation logic to execute on the processor nodes; providing switch emulation logic to execute on the switch node; establishing a first set of virtual interfaces with the non-Ethernet switch fabric, said first set of interfaces being between the switch emulation logic on the switch node and each processor node, wherein each virtual interface of the first set defines an indirect software communication path from one processor node to another processor node via the non-Ethernet switch fabric and via the switch node; establishing a second set of virtual interfaces with the non-Ethernet switch fabric, said second set of interfaces being between each processor node and every other processor node, wherein each virtual interface of the second set defines a direct

software communication path from one processor node to another processor node via the non-Ethernet switch fabric while avoiding the switch node; if a virtual interface from the second set of interfaces is operating to satisfy predetermined criteria, the Ethernet driver emulation logic of the one processor node unicast communicating with the other processor node via the virtual interface from the second set of interfaces; and if the virtual interface from the second set of interfaces is operating to not satisfy predetermined criteria, the Ethernet driver emulation logic of the one computer processor node unicast communicating with the other processor node via a virtual interface from the first set of interfaces. *Aditya substantially teaches* providing Ethernet driver emulation logic to execute on the processor_nodes (*fig.2 (126); col.1 line 14-col.2 line 37)*; providing switch emulation logic to execute on the switch node *(fig.1 (150), col.1 line 14-col.3 line 6*); establishing a first set of virtual interfaces with the non-Ethernet switch fabric, said first set of interfaces being between the switch emulation logic on the switch node and each processor node, wherein each virtual interface of the first set defines an indirect software communication path from one processor node to another processor node via the non-Ethernet switch fabric and via the switch node (*col.1 line 56-col.2 line 6*); establishing a second set of virtual interfaces with the non-Ethernet switch fabric, said second set of interfaces being between each processor node and every other processor node, wherein each virtual interface of the second set defines a direct software communication path from one processor node to another processor node via the non-Ethernet switch fabric while avoiding the switch node (*col.1 line 14-col.2 line 62, also col.5 line 61-col.6 line 45*); if

a virtual interface from the second set of interfaces is operating to satisfy predetermined criteria, the Ethernet driver emulation logic of the one processor node unicast communicating with the other processor node via the virtual interface from the second set of interfaces (*fig.8, col.6 line 50-col.7 line 28*); and if the virtual interface from the second set of interfaces is operating to not satisfy predetermined criteria, the Ethernet driver emulation logic of the one computer processor node unicast communicating with the other processor node via a virtual interface from the first set of interfaces (*fig.8, col.6 line 50-col.7 line 28*). It would have been obvious to one ordinary skilled in the art at the time of the applicant's invention to combine the teachings of Cox et al with Aditya for the purpose of directing data traffic throughout the network. Also Cox et al. teaches the use of an arithmetic logic within a microprocessor (*see col.9 lines 19-51*). Furthermore, Aditya teaches the advantage of reducing overflow and data ordering problems (*see col.6 lines 46-61).*

4.2. As per claims 2 and 12, the combined teachings of Cox et al. and Aditya substantially teach that wherein each of the processor nodes is associated with a virtual MAC address wherein the MAC addresses are formed according to rules to identify the computer processor acting as the processor node distinct from that of the external network (*see Aditya col.3 line 46-col.5 line 60; also see Cox et al. col.7 line 7-col.9 line 18*).

4.3. With regards to claims 3 and 13, the combined teachings of Cox et al. and Aditya substantially teach that the platform is connected to an external network via interface logic for communicating with an external network interface is associated with

its own MAC address, and wherein messages are communicated on the external network using the MAC address of the external network interface logic (*see Aditya col.4 line 61-col.6 line 45)*.

4.4. With regards to claims 4 and 14, the combined teachings of Cox et al. and Aditya substantially teach a first processor node uses a first virtual interface to unicast communicate with a second processor node but wherein the second processor uses a different virtual interface to communicate to the first processor node (*see Aditya fig.1-3 col.3 line 46-col.6 line 45; also col.1 lines 60-62*); *also see Cox et al. col.1 line 23-col.4 line 25)*.

4.5. As per claims 9 and 19, the combined teachings of Cox et al. and Aditya substantially teach the switch emulation logic that defines and maintains computer processor membership (*see Aditya col.5 line 31-col.6 line 60, also see Cox et al. col.7 line 7-col.8 line 8)*.

5.0 Claims 5-7 and 15-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cox et al., in view of Aditya, as applied to claims 1-4,9 and 11-14,19 above, and further in view of Hebert (U.S. Patent No. 6,728,780).

5.1. In considering claims, 5 and 15, Cox et al., as modified by Aditya, teach most of the instant invention and particularly teaches the check summing capability (*fig. 6 col. 5 lines 38-43*); however, he does not teach the disabling of such check summing. Hebert teaches the disabling of such check summing if the switch fabric driver logic has already check summed a message (see Hebert col.2 lines 51-59). It would have been to one ordinary skill of the art to combine the teachings of Cox et al., as modified by Aditya

with Herbert for the purpose of disabling check-summing capability so that the system does not check sum a message that has already been check summed. Herbert further teaches the advantage of minimizing network interruption and automating service of network problems by portable switches across multiple platforms (col.2 lines 32-49).

5.2. With regards to claims 6 and 16, the combined teachings of Cox et al., Aditya and Herbert teach the switch fabric driver logic implements a reliable communication protocol to insure reception of messages over the switch fabric (see *Hebert col.5 lines 12-17; also Cox et al. title, abstract, and col.1 line 23-col.4 line 25).*

5.3. With regards to claims 7 and 17, the combined teachings of Cox et al., Aditya, and Hebert teach the redundant configuration (*see Hebert figure 3 col. 4 lines 56-57*).

6. Claims 8,10, 18 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cox et al. in view of Aditya, as applied to claims 1-7,9 and 11-17,19 above, and further in view of Trachewsky et al (U.S. Patent No. 6,898,204).

6.1. With regards to claims 8 and 18, Cox et al., as modified by Aditya, teaches most of the instant invention and particularly teaches broadcast communicates messages (see Cox et al. col.1 line 23-col.4 line 25); also *see Aditya figures 3-5*); however it does not expressly teach receiving and cloning the broadcast message from the virtual interface and transmitting it to the other computer processors in the network. Trachewsky et al substantially teaches the use of an Ethernet emulation logic to broadcast communicate a message by sending the message to the switch emulation logic via a virtual interface as the switch emulation logic receives and clones the

broadcast message from a virtual interface and transmits it the other computer processors in the network (*col.29 line 60 through col.30 line 58*). it would have been obvious to one ordinary skill in the art at the time of applicant's invention to combine the teaching of Cox et al., Aditya, and Trachewsky et al. in other to obtain a system capable of intercepting and/or retrieving these broadcast messages and routing them to other computer processors in the network. Trachewsky et al. further teaches the improvement of transmission performance in a frame-based communication network (col.1 lines 14-44) and the improvement of LAN delivery latency (col.97 lines 24-38).

6.2. As per claims 10 and 20, the combined teachings of Cox et al., Aditya and Trachewsky et al teach the transmission capability of a switched Ethernet driver emulation logic of more than the maximum transmission unit (MTU) (see *Trachewsky et al col. 29 line 60 through col.31 line 10).*

Conclusion

7.0 The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

7.1 Gessel et al. (U.S. Patent No. 5,889,954) teaches a network manager for configuring and controlling a simulated telecommunications network having a plurality of nodes, which communicates in a plurality of communication protocols.

7.2 Shue et al. (U.S. Patent No. 6,862,564) teaches a system and method for providing an emulated network including a plurality of emulated networking devices, in which a number of network nodes executable images are employed.

7.3 McLain et al. (U.S. Patent No. 6,295,518) teaches a system and method for emulating telecommunication network devices.

7.4 Von Hammerstein (U.S. Patent No. 6,292,495) teaches a an apparatus and method for communicating link status information for permanent virtual circuit that shared a data link connection identifier.

7.5 Lasserre (USPG_PUB No. 2002/0174251) teaches a method and system for connecting virtual circuit across an Ethernet switch.

8.0 Claims 1-20 are rejected and applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

8.1 Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andre Pierre-Louis whose telephone number is 571-272-8636. The examiner can normally be reached on Mon-Fri, 8am-4: 30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Leo P. Picard can be reached on 571-272-3749. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

January 6, 2006

APL

Paul L. Rodriguez 1/6/06

Primary Examiner
Art Unit 2125